

WHAT IS CLAIMED IS:

1. A metal oxide semiconductor transistor comprising:
 - a semiconductor substrate;
 - a source area formed in a device area of the semiconductor
 - 5 substrate;
 - a drain area formed in the device area;
 - a gate layer formed on and across the device area between the
 - source area and the drain area;
 - a control gate layer having a first part including a first end of the
 - 10 control gate layer and a second part including a second end of the
 - control gate layer, the first part being formed on the device area
 - between the gate layer and at least one of the source area and the
 - drain area, the first end being disposed so that there is a gap between
 - the first end and an edge of the device area; and
 - 15 a diffusion area formed in the device area between the gate
 - area and the control gate area.
2. The metal oxide semiconductor transistor according to claim 1,
 - wherein the gate layer and the control gate layer are formed on a
 - 20 common plane.
3. The metal oxide semiconductor transistor according to claim 1,
 - wherein the second part is disposed outside the device area.

4. The metal oxide semiconductor transistor according to claim 1,
wherein

the second part is formed on the device area between the drain
area and the gate layer, and

5 the second end is disposed so that there is a gap between the
second end and an edge of the device area.

5. The metal oxide semiconductor transistor according to claim 1,
wherein

10 the gate layer has outside the device area a first contact area
connected to an electrode,

the gate control layer has outside the device area a second
contact area connected to an electrode, and

15 the first contact area and the second contact area are disposed
in one side of the device area.

6. The metal oxide semiconductor transistor according to claim 1,
wherein

20 the gate layer has outside the device area a first contact area
connected to an electrode,

the gate control layer has outside the device area a second
contact area connected to an electrode, and

the first contact area is opposite to the second contact area with
respect to the device area.

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7. The metal oxide semiconductor transistor according to claim 1,
wherein

the second part is formed on the device area between the
source area and the gate layer,

5 the second end is disposed so that there is a gap between the
second end and the first end, and

the control gate layer has a third part connecting the first part
and the second part outside the device area.

10 8. The metal oxide semiconductor transistor according to claim 1,
wherein the diffusion area includes an impurity with same conduction
type as the source area and the drain area, and has an impurity
concentration lower than an impurity concentration in the source area
and the drain area.

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9. A metal oxide semiconductor transistor comprising:

a semiconductor substrate;

a source area formed in a device area of the semiconductor
substrate;

20 a drain area formed in the device area;

a gate layer formed on and across the device area between the
source area and the drain area; and

a control channel area formed in the device area between the
gate layer and at least one of the source area and the drain area, the

25 control channel area having a threshold value that gradually changes in

a longitudinal direction of the gate layer.

10. The metal oxide semiconductor transistor according to claim 9,
further comprising a second control channel area formed in the device
5 area between the gate layer and at least one of the source area and the
drain area, wherein

the control channel area between the gate layer and at least one
of the source area and the drain area has a threshold value that
gradually increases in the longitudinal direction, and

10 the second channel area has a threshold that gradually
decreases in the longitudinal direction.

11. The metal oxide semiconductor transistor according to claim 9,
wherein the control channel area includes a channel diffusion area that
15 has an impurity concentration that gradually changes in the longitudinal
direction.

12. The metal oxide semiconductor transistor according to claim 9,
further comprising an insulating layer formed on the control channel
20 area, the insulating layer having a thickness that gradually changes in
the longitudinal direction.